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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,319	02/09/2005	Farid N. Najm	361007-000043	6437

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EXAMINER	
KING, DOUGLAS	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/524,319	NAJM ET AL.	
	Examiner	Art Unit	
	Douglas King	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-5 and 9-13* is/are allowed.

6)☒ Claim(s) *1,2 and 6-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9 February 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *East Search, Plus Search*.

DETAILED ACTION

Information Disclosure Statement

1. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 9 February 2005. The information disclosed therein was considered.

Drawings

2. Figures 1 and 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because the operation of the sense amplifier of Figure 14 in view of the specification (pages 16-17) is unclear. It appears that the output nodes A and B should be conductively connected to nodes between transistors P1, N1 and P2, N2 respectively. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as

"amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 3, 9, and the claims which depend therefrom (4,5,10-13) are objected to because of the following informalities. In claim 3 lines 27-34 refer to "a first pair of cross coupled inverters across a bitline (BL) and a bitline bar (BLB)" and later to a "second pair of cross couple inverters." According to the embodiment of figure 14 (see objection above) and to the specification regarding the sense amplifier it is unclear as to whether the described devices function as inverters. Appropriate correction is required.

5. Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1, 2, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamauchi (USPGPUB 2003/0002328).**

Regarding independent claim 1, Yamauchi discloses an asymmetric SRAM cell (see paragraph 8) for storing a binary variable, the asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell (see paragraphs 28 and 36) when the asymmetric SRAM cell stores a binary variable representing a predetermined binary value (a "low" value, for example), the asymmetric SRAM cell comprising: a plurality of transistors (Figure 1, elements MN0-MN3, MP0, and MP1) operably coupled and configured as an asymmetric SRAM cell (see paragraph 8), wherein the plurality of transistors include at least one first type of transistor (Figures 1 and 2, transistor MN1) and at least one second type of transistor (Figures 1 and 2, transistor MN0) that is weaker than the first type of transistor (Figure 2, second transistor MN0 has higher threshold voltage and smaller gate (channel) width than first transistor MN1), such that the configuration of the asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only (see paragraphs 28 and 36).

Regarding dependent claim 2, Yamauchi discloses the asymmetric SRAM cell of claim 1 wherein at least one of the second type of transistor is a transistor having a higher voltage threshold as compared to the voltage threshold of the first type of transistor (see Figures 2 and 3, where MN1 is the first type and MN0 is the second type). Yamauchi further discloses the asymmetric SRAM cell of claim 1 wherein at least one of the second type of transistor is a transistor having a decreased channel width as

compared to the channel width of the first type of transistor (see Figures 2 and 3, gate width).

Regarding independent claim 6, Yamauchi discloses an SRAM device comprising an array of SRAM cells (in paragraph 1 "memory cells can be arranged" implies a plurality of arranged memory cells) wherein each SRAM cell stores a binary variable representing a predetermined binary value (a "low" value for example) , and each SRAM cell is an asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell (see paragraphs 28 and 36 in view of the plurality of cells described in paragraph 1) each asymmetric SRAM cell comprising: a plurality of transistors (Figure 1, elements MN0-MN3, MP0, and MP1) operably coupled and configured as an asymmetric SRAM cell (see paragraph 8), wherein the plurality of transistors include at least one of a first type of transistor (Figures 1 and 2, transistor MN1) and at least one second type of transistor (Figures 1 and 2, transistor MN0) that is weaker than the first type of transistor (Figure 2, second transistor MN0 has higher threshold voltage and smaller gate (channel) width than first transistor MN1), such that the configuration of the asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only (see paragraphs 28 and 36).

Claim Rejections - 35 USC § 103

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamauchi (USPGPUB 2003/000232^) in view of Meyer (US Patent No. 6,425,056).

Regarding claims 7 and 8, Yamauchi discloses the SRAM device of claim 6 but does not explicitly disclose that the asymmetric SRAM cell device comprise an SRAM device selected from the group consisting of a direct store SRAM device or a selectively inverted SRAM device as in claim 7. Further, Yamauchi does not disclose that the SRAM device comprises a cache memory selected from the group consisting of a direct store cache memory and a selectively inverted cache memory as in claim 8. However, Meyer teaches the direct store (called direct mapped by Meyer) cache memory may include any of a wide-variety of suitable high-speed memory devices, particularly SRAM memory (Meyer, column 4 lines 7-12, and column 2 lines 49-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the asymmetric SRAM array of Yamauchi in the direct store cache as taught by Meyer, for the benefit of reducing current leakage (see Yamauchi paragraphs 8 and 28).

Allowable Subject Matter

8. Claims 3-5 and 9-13 would be allowable if rewritten to overcome the objections state in above paragraph 4.

Regarding independent claim 3, the following is an examiner's statement of reasons for allowance: there is no teaching or suggestion in the prior art of a sense amplifier for coupling with an asymmetric SRAM for providing faster access times comprised of: two pairs of cross-coupled inverters; a dummy column of cells storing a predetermined binary value at all times wherein during a read operation, said dummy column is operably coupled with the first pair of cross-coupled inverters; four input lines, a bitline (BL) and a bitline bar (BLB) input from the asymmetric SRAM cell and a dummy

bitline (D) and dummy bitline bar input from the dummy column, wherein the dummy bitline is input to the sense amplifier on the same side as the bitline bar and the dummy bitline bar is input to the sense amplifier on the same side as the bitline.

Regarding independent claim 9, the following is an examiner's statement of reasons for allowance: there is no teaching of suggestion in the prior art of a combination asymmetric SRAM device and sense amplifier for coupling with said SRAM device for wherein at least one sense amplifier is comprised of: two pairs of cross-coupled inverters; a dummy column of cells storing a predetermined binary value at all times wherein during a read operation, said dummy column being operably coupled with the first pair of cross-coupled inverters; four input lines, a bitline (BL) and a bitline bar (BLB) from the asymmetric SRAM cell and a dummy bitline (D) and dummy bitline bar from the dummy column, wherein the dummy bitline is input to the sense amplifier on the same side as the bitline bar and the dummy bitline bar is input to the sense amplifier on the same side as the bitline.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Naffziger et al., U.S. PGPUB 2001/0043486; Yokozeki, U.S. Patent No. 6,556,472; Zhang et al., U.S. Patent No. 5,949,256.

Naffziger teaches a SRAM cell wherein the transistors are asymmetric in size.

Yokozeki teaches the use of dummy cells for the timing of memory read operations.

Zhang teaches an asymmetric sense amplifier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas King whose telephone number is (571) 272-2311. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DSK

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